國立臺東大學在積體電路設計教育創新與實踐之研究

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摘要

近年來全球半導體產業快速發展，凸顯出積體電路（IC）設計人才日益迫切的需求。台灣雖在全球半導體製造中扮演關鍵角色，然在IC設計教育中，學術理論與產業實務間的落差依然是一大挑戰。位於台灣東部的國立臺東大學（NTTU）相較於台灣西部大學資源匱乏，近年來仍致力推廣積體電路設計課程，採取漸進模組式和專題導向的教學模式來推動IC設計教育。本研究探討NTTU在積體電路設計晶片教育創新與實踐之研究。

首先，NTTU必須與國家實驗研究院台灣半導體研究中心(TSRI)和台灣積體電路製造股份有限公司(TSMC)三方首次共同簽署合約。其次，簽約完成後方能使用台灣半導體研究中心IC設計軟體，學生必須一步一步依循整套IC設計流程來設計電路。接著，學生晶片設計完成後，必須通過台積電製程部門所設下的驗證關卡。最後，學生IC設計通過驗證後方能下線，請台積電製作晶片。晶片製作完成後，學生必須量測晶片功能，驗證與其當初設計電路功能是否一致。

NTTU 可以整合基礎課程、軟體模擬與專題製作導向學習的漸進式教學模式，讓學生使用台積電 180 奈米製程，從電路設計、電路前模擬、電路佈局、DRC 驗證、LVS 驗證、寄生效應萃取、電路後模擬，最後下線請台積電製作晶片。NTTU 已發展出適合學生背景的 IC 設計培育方法，並提出一套可持續且具擴展性的半導體 IC 設計人才培育模式。

關鍵字: 積體電路設計、國立臺東大學、晶片製作、半導體高等教育

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A Study on Innovation and Implementation in Integrated Circuit Design Education at National Taitung University

Chih-Lung Tseng*

Abstract

In recent years, the rapid development of the global semiconductor industry has underscored the growing demand for skilled professionals in integrated circuit (IC) design. Although Taiwan plays a key role in the global semiconductor manufacturing landscape, a significant gap remains between academic theories and industrial practices in IC design education. Located in eastern Taiwan and comparatively under-resourced relative to universities in the western region, National Taitung University (NTTU) has made consistent efforts in promoting IC design education. The university has adopted a progressive, modular, and project-based teaching approach to bridge the gap between theory and practice.

This study explores NTTU's innovation and implementation in IC design chip education. First, NTTU must sign a tripartite agreement for the first time with the National Applied Research Laboratories Taiwan Semiconductor Research Institute (TSRI) and Taiwan Semiconductor Manufacturing Company (TSMC). Following the agreement, NTTU gained access to IC design software provided by TSRI, allowing students to follow the complete IC design flow step by step. After completing their chip designs, students must pass verification procedures established by TSMC's fabrication division. Finally, only upon successful verification can the designs proceed to tape-out and fabrication by TSMC. Once the chips are produced, students are required to test and validate the functionality of their chips to ensure consistency with their original circuit designs.

NTTU has developed an integrated, progressive instructional model that combines fundamental course, software simulation, and project-based learning. Using TSMC's 180nm process technology, students can participate in the entire IC design process, including schematic design, pre-simulation, circuit layout, design rule checking (DRC), layout vs schematic (LVS) verification, parasitic extraction and post-simulation, ultimately completing tape-out and chip manufacturing. Through these efforts, NTTU has established an integrated IC design training model based on the student background, and proposed a sustainable and scalable talent training model for the semiconductor IC design field.

Keywords: Integrated Circuit (IC) Design, National Taitung University (NTTU), Chip Manufacturing, Semiconductor Higher Education.

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Introduction

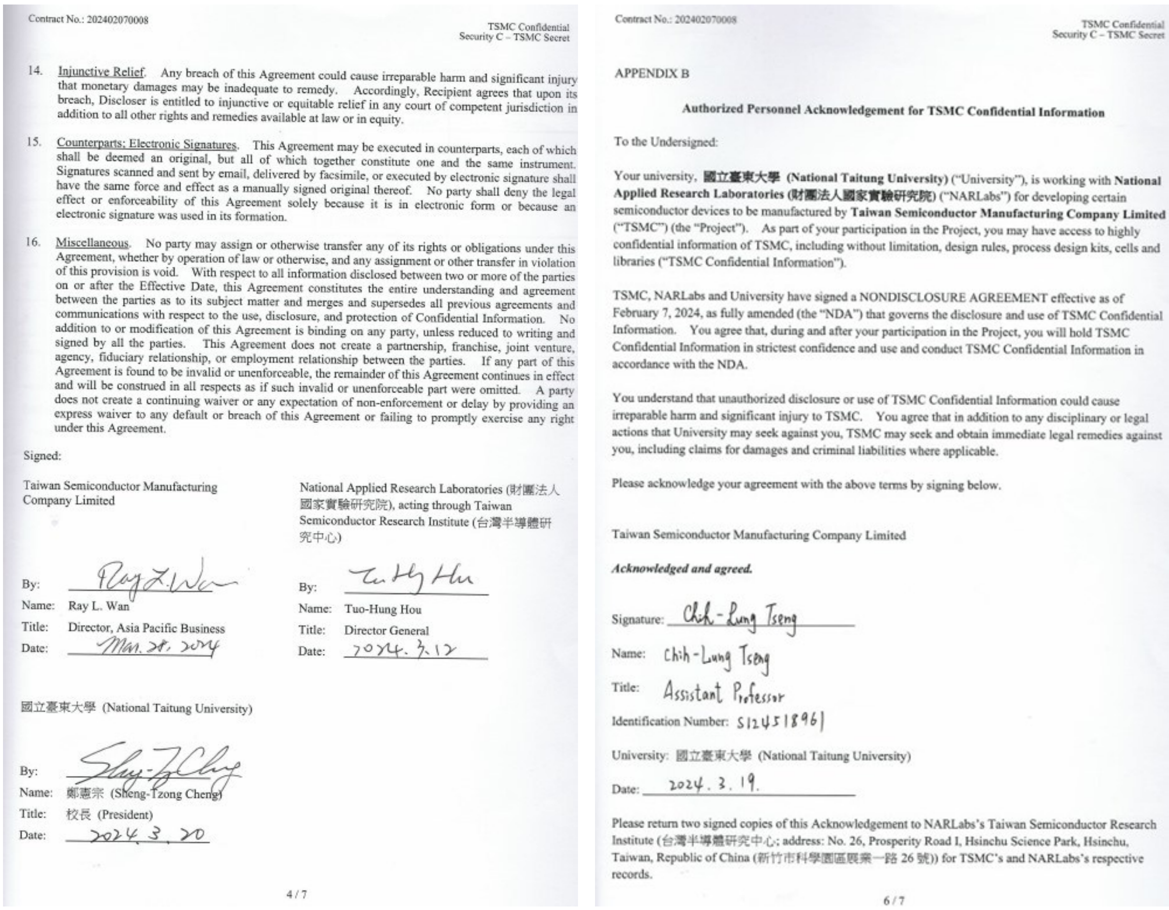
The development of integrated circuit (IC) design has become a cornerstone of technological innovation and economic competitiveness. The IC industry now lies at the heart of modern electronic devices, with applications spanning mobile phones, wearable devices, artificial intelligence (AI), and even quantum computing systems (Chiang & Kuo, 2021). Taiwan holds a leading position in global semiconductor manufacturing and design, home to world-renowned companies such as Taiwan Semiconductor Manufacturing Company (TSMC), MediaTek Inc., and Realtek Semiconductor Corporation. Despite these technological advances, cultivating IC design talent remains a challenge, especially at universities in remote areas with limited resources. While top-tier institutions such as National Yang Ming Chiao Tung University and National Taiwan University have established comprehensive IC research systems and foster strong industry collaborations, regional universities like National Taitung University (NTTU) face significant obstacles. These problems include limited laboratory facilities, small number of professional teachers, and large gaps in students' basic knowledge.

According to Lin and Hsieh (2022), the modular integration of circuit design support tools can help mitigate resource constraints while maintaining high teaching quality. Many studies have emphasized the importance of practice-oriented IC design education that aligns closely with industry needs. For instance, Chiang and Kuo (2021) found that project-based learning significantly enhances student engagement and technical proficiency in VLSI courses. Moreover, Su and Chen (2020) highlighted the need for localized course development tailored to students' diverse backgrounds and regional resource limitations. International studies also support diversified models of IC design education. For example, Ahmed and Riaz (2021) demonstrated that hybrid learning platforms combining simulation tools and remote laboratories improve both course accessibility and student engagement. These findings confirm the value of adaptive and context-sensitive educational strategies.

As Taiwan to lead the global semiconductor industry, extending IC education to non-metropolitan regions becomes increasingly vital. As Taiwan to lead the global semiconductor industry, extending IC education to non-metropolitan areas becomes increasingly important. In eastern Taiwan, NTTU has taken the initiative to implement a localized IC course designed specifically for students with limited access to resources. In recent years, NTTU has worked to bridge the gap between academic theory and industrial practice—not only addressing talent cultivation shortfalls but also responding to the needs of regional development by providing students with access to high-value knowledge aligned with national semiconductor strategies (Ministry of Education, 2022; National Development Council, 2023).

Figure 1 shows a major milestone in 2024, when NTTU signed its first tripartite agreement with the National Applied Research Laboratories Taiwan Semiconductor Research Institute (TSRI) and Taiwan Semiconductor Manufacturing Company (TSMC). This agreement, which includes confidentiality clauses regarding TSMC process technologies and silicon intellectual property, marked the starting point of NTTU's IC design education initiative. Leveraging TSRI's IC design software and TSMC's chip fabrication capabilities, NTTU adopted a progressive, modular, and project-based teaching model to promote IC design education. Departing from traditional lecture-based instruction, NTTU emphasizes hands-on circuit verification in its foundational electronics and circuit theory courses. This pedagogical approach aligns with national policies promoting localized semiconductor education and encourages regional universities to participate in Taiwan's innovation-driven economy (Lin & Hsieh, 2022).

This paper explores NTTU's instructional strategies, implementation outcomes, and potential in the field of IC design education. It also offers recommendations for future educational innovation and the development of sustainable semiconductor talent cultivation programs.



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14. Injunctive Relief. Any breach of this Agreement could cause irreparable harm and significant injury that monetary damages may be inadequate to remedy. Accordingly, Recipient agrees that upon its breach, Discloser is entitled to injunctive or equitable relief in any court of competent jurisdiction in addition to all other rights and remedies available at law or in equity.

15. Counterparts; Electronic Signatures. This Agreement may be executed in counterparts, each of which shall be deemed an original, but all of which together constitute one and the same instrument. Signatures scanned and sent by email, delivered by facsimile, or executed by electronic signature shall have the same force and effect as a manually signed original thereof. No party shall deny the legal effect or enforceability of this Agreement solely because it is in electronic form or because an electronic signature was used in its formation.

16. Miscellaneous. No party may assign or otherwise transfer any of its rights or obligations under this Agreement, whether by operation of law or otherwise, and any assignment or other transfer in violation of this provision is void. With respect to all information disclosed between two or more of the parties on or after the Effective Date, this Agreement constitutes the entire understanding and agreement between the parties as to its subject matter and merges and supersedes all previous agreements and communications with respect to the use, disclosure, and protection of Confidential Information. No addition to or modification of this Agreement is binding on any party, unless reduced to writing and signed by all the parties. This Agreement does not create a partnership, franchise, joint venture, agency, fiduciary relationship, or employment relationship between the parties. If any part of this Agreement is found to be invalid or unenforceable, the remainder of this Agreement continues in effect and will be construed in all respects as if such invalid or unenforceable part were omitted. A party does not create a continuing waiver or any expectation of non-enforcement or delay by providing an express waiver to any default or breach of this Agreement or failing to promptly exercise any right under this Agreement.

Signed:

Taiwan Semiconductor Manufacturing Company Limited

By:
Name: Ray L. Wan
Title: Director, Asia Pacific Business
Date: Mar. 28, 2024

National Applied Research Laboratories (財團法人國家實驗研究院), acting through Taiwan Semiconductor Research Institute (台灣半導體研究中心)

By:
Name: Tuo-Hung Hou
Title: Director General
Date: 2024. 3. 12

國立臺東大學 (National Taitung University)

By:
Name: 鄭憲宗 (Sheng-Tzong Cheng)
Title: 校長 (President)
Date: 2024. 3. 20

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APPENDIX B

Authorized Personnel Acknowledgement for TSMC Confidential Information

To the Undersigned:

Your university, **國立臺東大學 (National Taitung University)** ("University"), is working with **National Applied Research Laboratories (財團法人國家實驗研究院)** ("NARLabs") for developing certain semiconductor devices to be manufactured by **Taiwan Semiconductor Manufacturing Company Limited** ("TSMC") (the "Project"). As part of your participation in the Project, you may have access to highly confidential information of TSMC, including without limitation, design rules, process design kits, cells and libraries ("TSMC Confidential Information").

TSMC, NARLabs and University have signed a NONDISCLOSURE AGREEMENT effective as of February 7, 2024, as fully amended (the "NDA") that governs the disclosure and use of TSMC Confidential Information. You agree that, during and after your participation in the Project, you will hold TSMC Confidential Information in strictest confidence and use and conduct TSMC Confidential Information in accordance with the NDA.

You understand that unauthorized disclosure or use of TSMC Confidential Information could cause irreparable harm and significant injury to TSMC. You agree that in addition to any disciplinary or legal actions that University may seek against you, TSMC may seek and obtain immediate legal remedies against you, including claims for damages and criminal liabilities where applicable.

Please acknowledge your agreement with the above terms by signing below.

Taiwan Semiconductor Manufacturing Company Limited

Acknowledged and agreed.

Signature: Chih-Lung Tseng
Name: Chih-Lung Tseng
Title: Assistant Professor
Identification Number: S124518961
University: 國立臺東大學 (National Taitung University)
Date: 2024. 3. 19.

Please return two signed copies of this Acknowledgement to NARLabs's Taiwan Semiconductor Research Institute (台灣半導體研究中心; address: No. 26, Prosperity Road I, Hsinchu Science Park, Hsinchu, Taiwan, Republic of China (新竹市科學園區展業一路 26 號)) for TSMC's and NARLabs's respective records.

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Figure 1. *National Taitung University (NTTU), Taiwan Semiconductor Research Institute (TSRI), and Taiwan Semiconductor Manufacturing Company (TSMC) signed a confidentiality agreement on TSMC's semiconductor process and intellectual property rights.*

Research Methods

1. Research Structure

This study adopts an action research methodology to explore the application of experiential learning in IC design education when faced with pedagogical challenges. The research centers on the design and implementation of an experiential learning-based instructional model, grounded in theoretical content from IC design textbooks and supported by practical training using computer server workstations. The objective is to examine how students' understanding of IC design theories evolves after participating in the experiential learning program and how they identify, address, and resolve problems encountered during the learning process. Particular attention is paid to how students develop conceptual thinking related to chip design and internalize circuit design knowledge, thereby strengthening cognitive retention. At the same time, the study also aims to foster professional growth among instructors.

Action research is a practice-oriented research methodology that encourages practitioners to adopt a reflective, inquisitive, and critical stance toward their own professional practices. It involves a systematic process of inquiry into real-world problems encountered in the classroom with the goal of finding strategic solutions. Through an iterative cycle of planning, implementation, reflection, revision, and re-implementation, this method seeks to improve existing conditions, enhance teaching practices, and promote educators' professional development and empowerment.

Figure 2 shows the action research cycle for IC design education. This study aims to explore the effectiveness and challenges of IC design education at NTTU. The research focuses on three major dimensions: course design, student learning experience, and project-based outcomes.

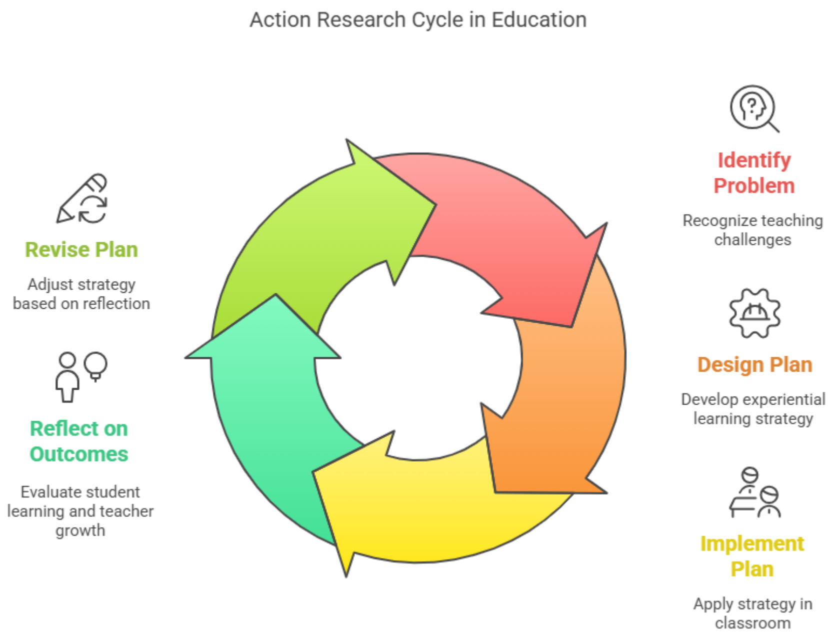


Figure 2. *IC design action research architecture diagram*

(1) Course Design Analysis

This study analyzes NTTU's IC design course, including its structure, learning objectives, teaching tools, and evaluation methods. The foundational courses include Electronics and Circuit Theory, while the core course, IC design, fully incorporates professional electronic design automation (EDA) tools such as Cadence Virtuoso.

(2) Student Learning Experience

The research evaluates the experiences of undergraduate and graduate students enrolled in IC-related courses through student satisfaction surveys. Additionally, selected students participated in semi-structured interviews to further investigate the challenges they faced, their motivations, and learning processes throughout the course.

(3) Evaluation of Project-Based Outcomes

Students' final project outcomes in the IC design course were assessed based on innovation, functional implementation, design complexity, and documentation quality. Furthermore, selected projects were benchmarked against academic standards and industry internship performances.

The action research methodology employed enables students to engage in systematic inquiry within real-world circuit design contexts. Through a continuous cycle of action and reflection, students remain actively involved in improving their designs to meet the requirements of tape-out fabrication. This cyclical process of research and practice strengthens their knowledge and expertise in IC design, ultimately providing a comprehensive representation of NTTU's educational reality in this domain.

2. Research Questions

This study is a form of action research conducted by the instructor within the teaching context. It primarily investigates both foundational and core courses related to IC design in the undergraduate and graduate programs. The objective is to integrate experiential learning into IC design education, thereby enhancing students' acquisition and application of professional knowledge in chip design. By collaborating with Taiwan Semiconductor Research Institute (TSRI) and Taiwan Semiconductor Manufacturing Company (TSMC), the study connects educational practices with local industry and regional development, fostering students' understanding of the value of chip design. Concurrently, the instructor continually reflects on and adjusts instructional practices to ensure the effectiveness of student learning outcomes in IC design education.

3. Scope of the Study

The study centers on courses related to IC design, specifically focusing on foundational courses such as Electronics and Circuit Theory, and the core course in IC design. The overall scope encompasses the innovation and practical implementation of chip design education at NTTU.

4. Experimental Subjects and Fields

(1) Experimental Subjects：

The primary participants are master's students from the Department of Green Energy and Information Technology, who enrolled in the IC design course. Undergraduate participants include second-year students taking Electronics and Circuit Theory, as well as third- and fourth-year students involved in capstone projects in the Department of Green Energy and Information Technology at NTTU.

(2) Experimental Fields：

The study was conducted in classrooms and computer workstation laboratories within the Department of Green Energy and Information Technology at NTTU. It was further extended through collaborative agreements with TSRI and TSMC, using IC design software provided by TSRI and chip fabrication support from TSMC.

5. Research Methods and Tools

The study adopts an action research methodology. During instructional practice, a diversified strategy of experiential learning was implemented to promote autonomous learning among students. Upon signing agreements with TSRI and TSMC, instructors were required to apply for user accounts, which students could only obtain through instructor verification. After acquiring accounts, permissions for EDA tool usage and IP registration were required, followed by process technology and intellectual property authorization applications. Due to TSMC's strict confidentiality policies regarding process technologies, all chip design work was conducted exclusively through secure online platforms.

Results and Discussion

Figure 3 shows the flowchart of the IC design process. The design begins with the specification of chip functionality, followed by a series of steps that systematically fulfill these functional requirements through circuit design. The IC design workflow consists of the following stages: defining chip functional requirements → circuit schematic design → pre-circuit simulation → layout design → design rule verification → parameter extraction → post-circuit simulation → chip fabrication.

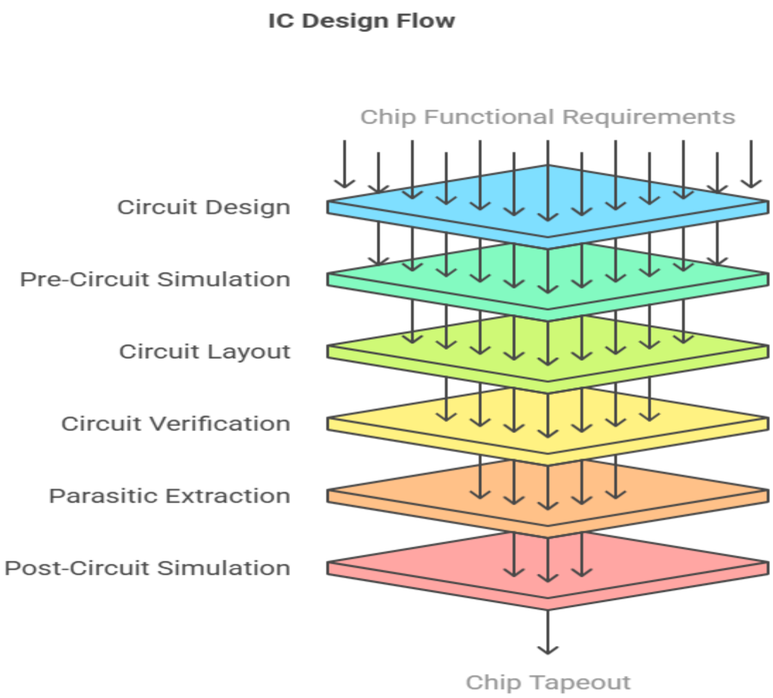


Figure 3. *IC design process flowchart*

Figure 4 shows a student-designed circuit schematic. The schematic drawing is a critical point in the IC design process, where the intended chip functionality is translated into a concrete circuit architecture. During this stage, students must determine the appropriate selection and functionality of various electronic components and represent them using standardized circuit symbols. These components are interconnected via wiring, which denotes the direction of current flow and the paths of signal transmission throughout the circuit.

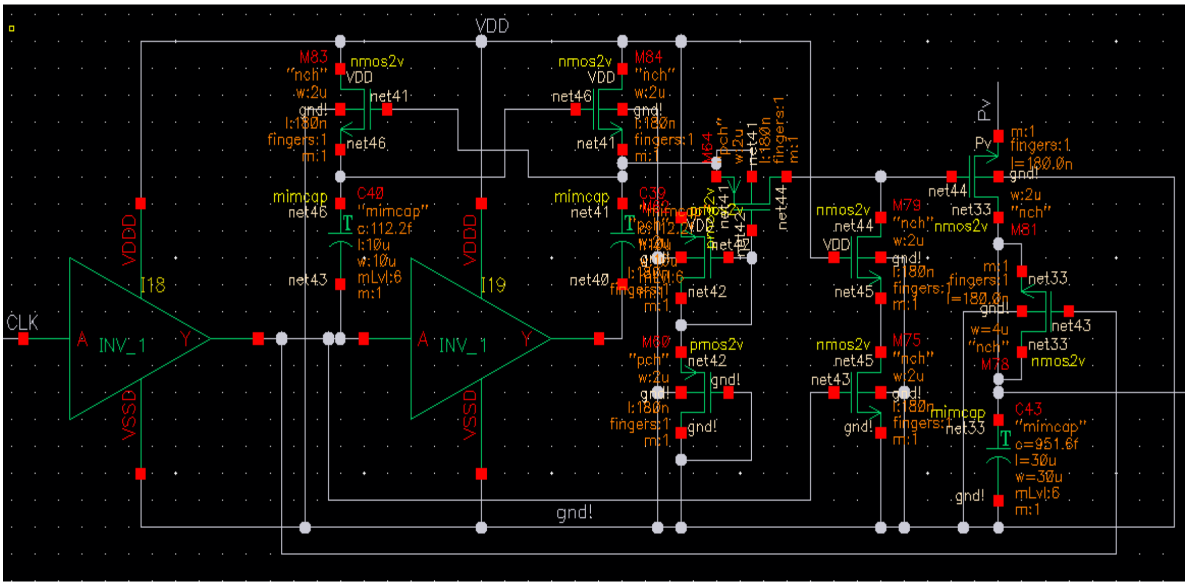


Figure 4. *Student-designed circuit schematic diagram*

Figure 5 shows a circuit simulation diagram created by a student. Once the circuit design is completed, a pre-circuit simulation is conducted to evaluate whether the design meets the specified functional requirements of the chip. The primary purpose of pre-circuit simulation is to predict and verify the behavior of the circuit before it proceeds to physical implementation. By using EDA tools, the circuit can be executed in a virtual environment to analyze its performance and behavior under various conditions. Such simulations typically include DC operating point analysis, frequency response analysis, and transient analysis. These analyses ensure the circuit performs reliably and stably across different operating conditions. The results from the pre-circuit simulation are instrumental in identifying potential design flaws early in the process, such as improper voltage biasing, signal distortion, or excessive power consumption. Detecting these issues in the early stages helps prevent costly errors during fabrication and testing. Through this process, the reliability and robustness of the circuit design are significantly enhanced, thereby improving the overall efficiency of the IC design workflow.

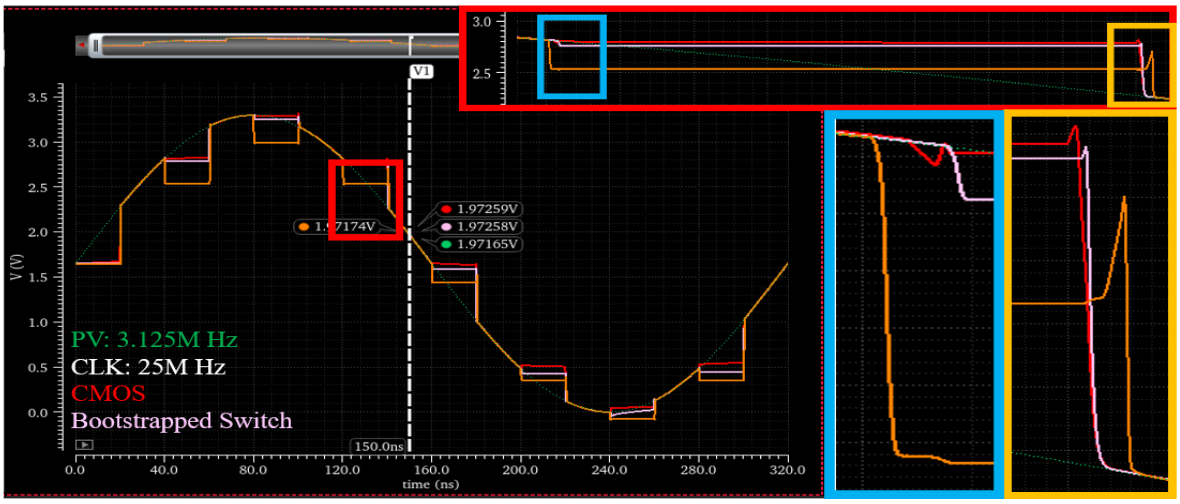
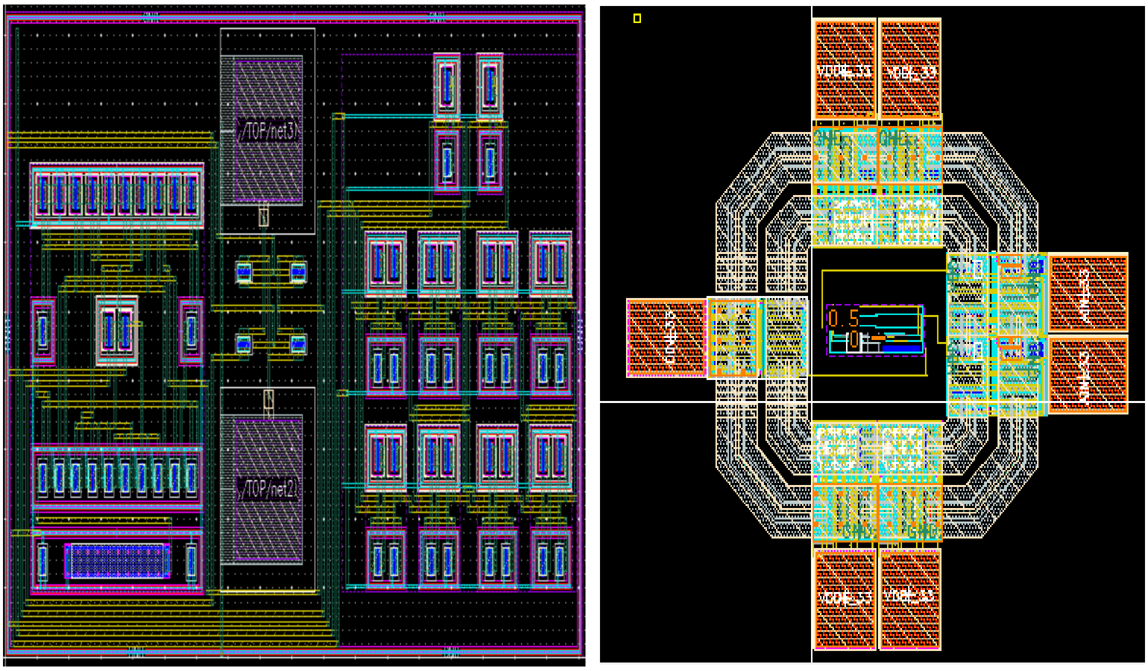


Figure 5. *Student-generated circuit simulation diagram*

Figure 6 shows student-generated circuit layout diagrams. Figure 6(a) shows the layout without I/O pad circuits, while Figure 6(b) includes the I/O pad circuits. While a circuit schematic provides a symbolic representation of an electronic circuit using simplified graphic symbols and interconnections of power and signal lines, it differs significantly from the actual physical layout required for fabrication. Therefore, once the schematic is completed, the next critical step is to proceed with the circuit layout design.

A circuit schematic typically comprises four main components: component symbols, interconnections, nodes, and annotations. The symbols represent actual electronic components, although their visual representations may differ from the physical appearance of real-world components. However, these symbols accurately convey essential attributes, such as the number and function of terminals.

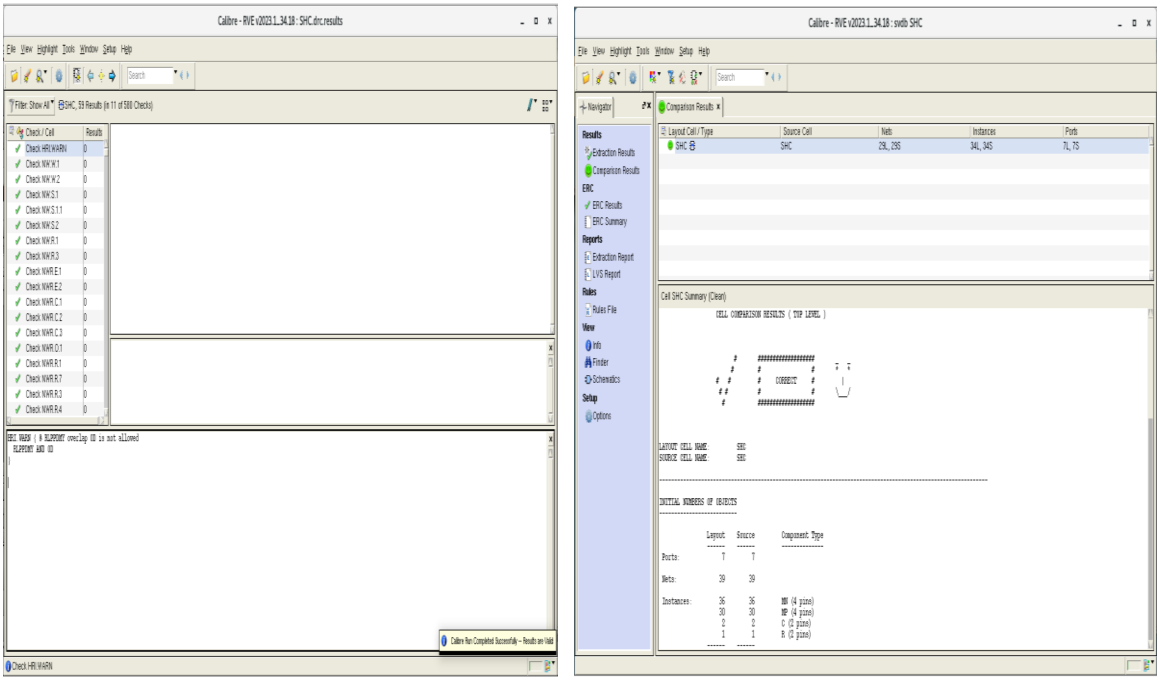
In layout design, although the schematic's functional requirements must be faithfully preserved, the physical implementation often demands adjustments and optimizations based on practical constraints such as area, performance, manufacturing process limitations, and parasitic effects. As a result, the layout is not a one-to-one reproduction of the schematic but rather a refined and implementable version tailored for fabrication and performance enhancement.



(a) (b)

Figure 6. *Student-generated circuit layout diagrams: (a) without I/O pad circuits and (b) with I/O pad circuits*

Figure 7 shows student-implemented circuit verification diagrams. Figure 7(a) shows a successful design rule check (DRC), while Figure 7(b) shows a successful layout versus schematic (LVS) verification. DRC is a critical step in the integrated circuit design flow, ensuring that the physical layout complies with the semiconductor manufacturing process constraints. DRC systematically examines the layout for violations of predefined geometric rules that, if unaddressed, could lead to fabrication failures or suboptimal device performance.



(a) (b)

Figure 7. *Student-generated circuit verification diagrams: (a) DRC passed and (b) LVS passed*

Typical DRC rules include constraints such as minimum line width, spacing between features, layer-to-layer distances, via dimensions, and other geometry-related limitations dictated by the process technology. DRC scans the entire layout and highlights any rule violations, enabling designers to detect and resolve issues prior to tape-out, thereby reducing manufacturing risks and associated costs. By ensuring conformance to fabrication specifications, DRC enhances the robustness of the design and minimizes the need for costly rework, ultimately shortening development cycles and optimizing production efficiency.

LVS verification complements DRC by confirming that the final physical layout accurately reflects the original schematic design. While DRC ensures that the layout meets geometric and process constraints, it does not verify the functional correctness or logical equivalence of the layout with the intended design. LVS addresses this gap by comparing the netlist extracted from the layout to the original schematic netlist, ensuring that connections, component instances, and circuit hierarchy are preserved. Together, DRC and LVS form the foundation of physical verification in IC design, safeguarding both manufacturability and functional integrity.

Once circuit verification is completed, layout parasitic extraction (LPE) is performed to quantify the impact of layout-induced parasitic elements on circuit behavior. This process is essential to ensure that the physical layout does not degrade the intended electrical performance. If the post-circuit simulation results fail to meet the original specifications, corrective actions must be taken. These may include circuit enhancement, parasitic analysis, or even redesigning both the schematic and the layout to meet performance requirements.

One of the major challenges at this stage is the inherent trade-off between minimizing chip area and managing parasitic effects. While layout designers strive to reduce chip size to optimize cost and integration density, aggressive area minimization can exacerbate parasitic capacitance and resistance, ultimately degrading circuit performance. Consequently, layout modification at this stage can be time-consuming and resource-intensive.

Following layout refinement, post-circuit simulation is conducted to validate the final circuit performance under realistic parasitic conditions. If the post-circuit simulation closely matches the results of the pre-circuit simulation, the design is deemed ready for tape-out. The completed design can then be submitted to the TSRI for fabrication via TSMC.

Conclusions

The findings of this study on the IC design course at NTTU hold significant implications for engineering education in remote areas. Three key themes emerged from the data: (1) localized and progressive course design, (2) the effectiveness of project-based learning, and (3) alignment with industry needs.

1. Localized and Scalable Course Design

The IC design course developed at NTTU demonstrates that a comprehensive and modern engineering education can be successfully implemented even in remote regions. The course progresses from basic circuit design and simulation to hands-on layout and verification, enabling students to develop both theoretical understanding and practical skills. This stepwise approach is particularly effective for students with limited prior knowledge, making it especially suitable for educational contexts in eastern Taiwan and other non-metropolitan areas.

2. Impact of Project-Based Learning

Project-based learning significantly enhanced students' motivation and self-confidence. Students reported that engaging in hands-on projects helped them understand real-world challenges in IC system design, such as workflow sequencing, debugging, and performance constraints. They also gained experience in teamwork and role allocation. These outcomes are consistent with constructivist learning theory and suggest that hands-on engagement should be central to technical education.

3. Alignment with Industry Demands

By incorporating industry-standard tools such as Cadence Virtuoso, the course equips students with practical competencies that enhance their employability and readiness for internships. Some students noted that their final projects were valuable assets during job interviews. Compared to resource-rich national universities, NTTU has leveraged intensive design practice to overcome geographic and resource limitations, illustrating that high-quality engineering education is not exclusive to elite institutions.

Acknowledgments

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